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***Research paper***

# On-Chip DC-DC Converter with High Ratio Conversion Voltage in 180nm CMOS Technology for Radio Frequency Identification Passive Tags

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***A b s t r a c t***

In this paper, a four-stage charge pump, which can be used on RFID tag chip, is presented in order to provide the desired voltage for the memory supply of the tag. In each stage of the proposed charge pump, one PMOS pass transistor, two switching MOSFET transistors and one capacitor are existed. The PMOS pass transistor is worked in sub-threshold region. The proposed charge pump circuit has high output voltage and conversion ratio. In the proposed charge pump, by choosing the input voltage about 1.8V, the output voltage, conversion ratio and power efficiency are achieved 8.9V, 98% and 85%, respectively. The designed charge pump circuit is simulated in 180nm CMOS technology with the help of Cadence software, while its chip area is 68µm×65µm.

***Keywords:***

*Charge pump,*
*DC-DC Converter,*
*RFID Tag,*
*Conversion Ratio,*
*Power Efficiency.*

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## 1. Introduction

In recent years the improvement of wireless communication technology is one of the important and challenging considerations. RFID is a wireless identification system, which transmits data between tag and reader with radio frequency waves [1]. Tag is a radio receiver-transceiver which is included one microchip and one antenna. Tag is categorized into three, active, passive and semi-passive groups. In contrast of active and semi-passive tags, which work with on-chip battery, passive tags attract more attention because of low fabrication cost and low chip area [2]. Passive tags are activated with emitted radio waves from reader. The supply management block of tag consists of rectifier, DC limiter and DC-DC converter. The tag antenna receives emitted RF waves from reader and these waves are converted to DC voltage with a rectifier. By increasing distance between tag and reader, input power and voltage of passive tag are decreased [2, 3]. Different parts of tag such as memory consisting of

ROM and RAM require higher voltages than the generated voltage from rectifier. Therefore a circuit should be inserted in supply management part of tag, in order to increase the regulator output voltage. To fulfil this requirement, DC-DC converter is used. The most common DC-DC converters are switched capacitor and charge pump circuits. Since switched capacitor converters need more chip area, they can't be suitable for RFID applications [4]. Most of presented charge pump circuits work based on Dickson charge pump [5]. The operation of Dickson charge pump is limited by drop voltage of $V_{TH}$, on the other hand, by drop voltage of $V_{TH}$ the circuit efficiency is decreased as a result of body effect of MOSFET transistors in higher stages. Sheng et al. [6], for overcoming body effect, used the improved diode-connected CMOS, in which the body of PMOS (NMOS) is connected to the highest (lowest) voltage of circuit dynamically. To gain higher efficiency in charge pump circuit, the more complicated circuits are presented. Lauterbach et al. [7] utilized the charge sharing concept for ameliorating the charge pump efficiency. Huang et al. [8] used the charge pump with only one clock signal instead of the two clock signals conventional charge pump. In the mentioned charge pump circuits, the more voltage has dropped in voltage transmission path from input to output, as charge transmission MOSFETs are activated. Thus the voltage conversion ratio is diminished, while the power consumption is increased. Hwang et al. [9] presented the charge pump which has 91.1% conversion ratio while its power efficiency is 62%. In this paper, a charge pump circuit is proposed for the purpose of high output voltage and low power consumption.

The paper is organized as follows: in section 2 Dickson charge pump is presented accurately. The designed charge pump is proposed in section 3 and the simulation results are provided in section 4. Finally, the whole work is concluded in section 5.

## 2. Dickson charge pump

The presented charge pump by Dickson, which is shown in Figure 1, is used extensively for generating higher voltages than input supply voltage [5]. The structure of the circuit consists of capacitors which are connected in parallel from by means of diodes.

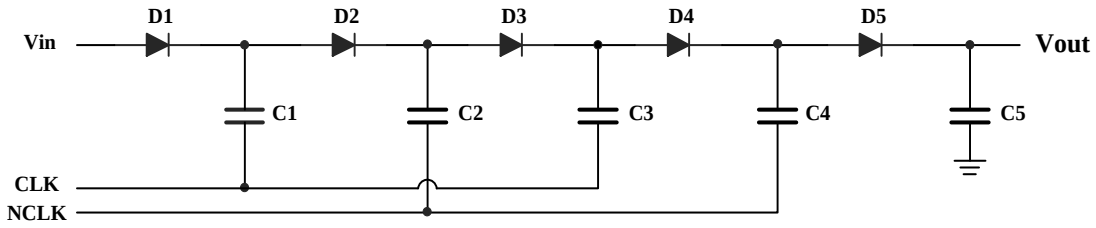


Fig.1: Dickson charge pump circuit

The output voltage of Dickson charge pump is calculated from (1).

$$V_{out,N} = N\left(V_{in} - V_D\right) \tag{1}$$

Where $V_{out, N}$ is the output voltage of N-th stage, N is the number of stages and $V_D$ is the voltage drop of each diode.

The usage of CMOS technology for fabrication is easier than silicon diodes. Therefore in Dickson charge pump, the diode connected MOSFET transistors are employed instead of silicon diodes, for charge transmission to the higher stages. The Dickson charge pump with NMOS transistors is shown in Figure 2. The charge pump includes two CLK and NCLK signals which work in opposite phases, while their amplitude equals to input voltage amplitude. The NMOS chain transistors, which are connected sequentially, operate as switches. With this mechanism, the output voltage is more than the input voltage.

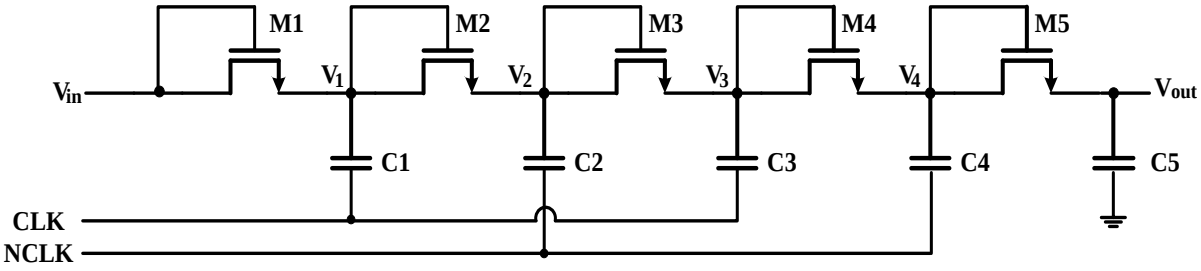


Fig.2: The four-stage charge pump with diode connected MOSFET

When the CLK becomes low, the $M_1$ MOSFET becomes on and $V_1$ is calculated based on (2).

$$V_1 = V_{in} - V_{TH} \tag{2}$$

Where $V_{TH}$ is the threshold voltage of MOSFET transistors. When the CLK changes into high, due to the same amplitude of CLK, NCLK signals and input voltage, $V_1$ is achieved from (3).

$$V_1 = V_{in} + V_{in} - V_{TH} \tag{3}$$

At this time the NCLK signal becomes low, which results in activating $M_2$ MOSFET. Thus $V_2$ is calculated from (4).

$$V_2 = \left(V_{in} + V_{in} - V_{TH}\right) - V_{TH} = 2\left(V_{in} - V_{TH}\right) \tag{4}$$

Consequently, the N-th stage output voltage of Dickson charge pump is gained from (5), while no load is employed.

$$V_{out,N} = N\left(V_{in} - V_{TH}\right) \tag{5}$$

### 3. The proposed charge pump

Figure 3 shows one stage of the proposed charge pump which includes two PMOS transistors, one NMOS transistor and one capacitor. The amplitude of CLK and NCLK signals is as same as input voltage amplitude which equals to $V_{DD}$.

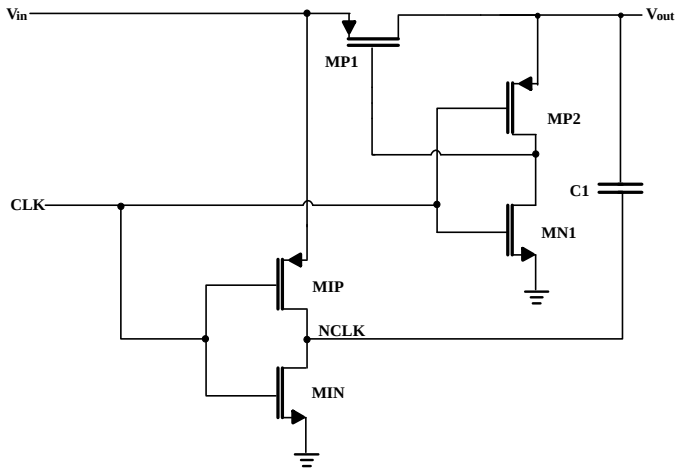


Fig.3: One stage of the proposed charge pump

Figure 4 shows CLK, NCLK and $V_{out}$ waveforms.

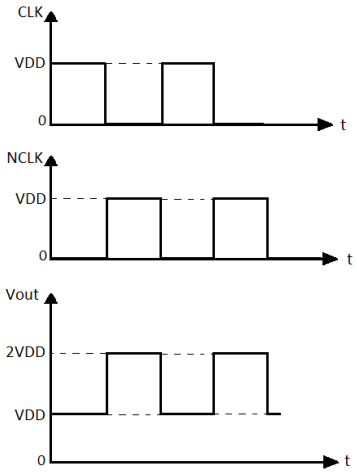


Fig.4: Input and output waveforms

In the first half-cycle, where the amplitude of CLK signal equals to $V_{DD}$, $M_{P1}$ and $M_{N1}$ are on, while $M_{P2}$ is in cut-off region. At first, the capacitor voltage is zero and $M_{P1}$ enters to saturation region.

In the second half-cycle, the amplitude of CLK signal becomes zero, $M_{P1}$ and $M_{N1}$ transistors go to cut-off region and $M_{P2}$ transistor is on. In this situation, the amplitude of NCLK signal reaches to $V_{DD}$, so it is expected that $V_{out}=2V_{DD}$. It should be noted that, in this analysis $M_{N1}$ and $M_{P2}$ transistors are considered as ideal switches. In the third half-cycle, the amplitude of CLK signal is equals to $V_{DD}$ for the second time. Given the fact that the voltage is stored in capacitor in previous process, $M_{P1}$ transistor enters to triode region and its drain current in this situation can be calculated from (6).

$$I_{tri} = K\left(V_{SG} - |V_{TP}|\right)V_{SD} \quad (6)$$

where $V_{SD}$ is the drain-source voltage of $M_{P1}$. As it is shown in Figure3, the output voltage of i-th period equals to (7).

$$V_{out} = \frac{\left(i - \frac{1}{2}\right)}{fC_1} I_{tri} \tag{7}$$

f is the operation frequency of CLK and NCLK signals and $I_{tri}$ is the triode region current of i-th period. The source-drain voltage of $M_{P1}$ is achieved from (8).

$$V_{SD} = V_{DD} - \frac{\left(i - \frac{1}{2}\right)}{fC_1} I_{tri} \tag{8}$$

By combination of (6) and (8), the triode region current is calculated from (9).

$$I_{tri} = \frac{k\left(V_{SG} - |V_{TP}|\right)V_{DD}}{1 + \frac{\left(i - \frac{1}{2}\right)}{fC_1} k\left(V_{SG} - |V_{TP}|\right)} \tag{9}$$

Therefore if $\frac{\left(i - \frac{1}{2}\right)}{fC_1} k\left(V_{SG} - |V_{TP}|\right) >> 1$, (8) can be approximated from (10).

$$V_{out} \approx V_{DD} \tag{10}$$

In steady state, $M_{P1}$ transistor is worked in sub-threshold region, which culminates in very low source-drain voltage of transistors. Therefore the proposed charge pump has higher voltage conversion ratio in compare with the other charge pump circuits. In order to increase the output voltage, five blocks of the proposed charge pump circuit are connected sequentially. The four-stage charge pump is shown in Figure 5. The NCLK signal is employed to the first and the third stages, while the CLK signal is employed to the second and the fourth stages. When the CLK signal equals to $V_{DD}$, the voltages of node 1 and node 3 reach to $V_{DD}$ and $3V_{DD}$, respectively. When CLK signal becomes low, the voltage of node 3 in the third- stage equals to $4V_{DD.}$ Finally, the output voltage is achieved $5V_{DD}$.

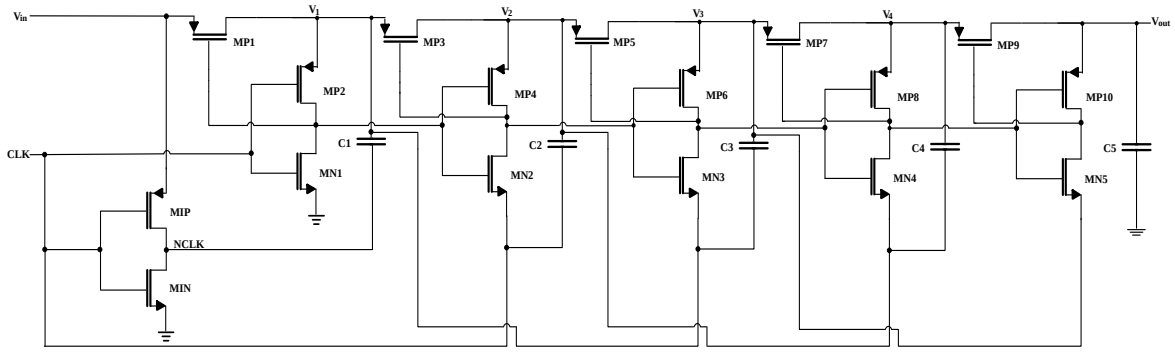


Fig.5: The proposed four-stage charge pump

## 4. Simulation results

In this section, for the purpose of proving the higher efficiency of the proposed design, Dickson charge pump shown in Figure 2, is simulated. Input voltage source and the amplitude of clock signals are considered 1 volt, while the clock signals frequency is set 1MHz. The output of each four-stage of Dickson charge pump and the proposed charge pump are shown in Figure 6 and Figure 7, respectively. The output voltages of Dickson charge pump and the proposed charge pump is 3.7V and 4.9V, respectively.

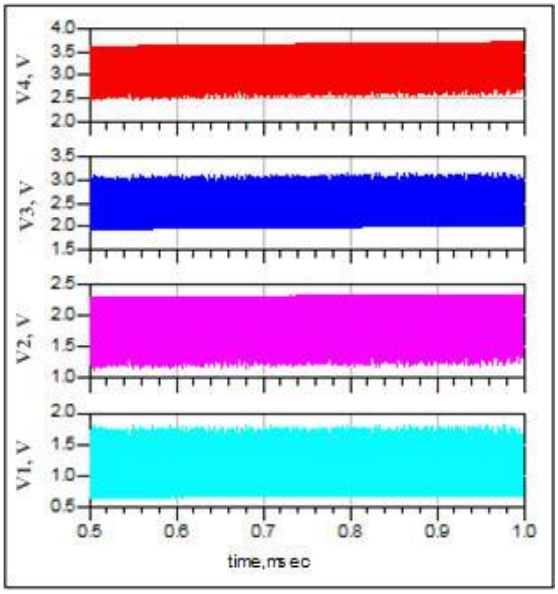


Fig.6: The voltage waveforms of Dickson charge pump stages

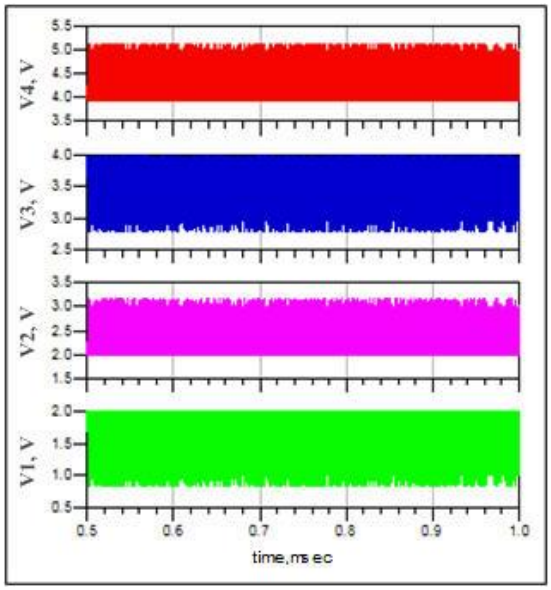


Fig.7: The voltage waveforms of the proposed charge pump stages

The output voltage of the proposed charge pump with CLK signal is shown in Figure 8. The output voltage of the designed charge pump is achieved 4.9 V in simulation results.

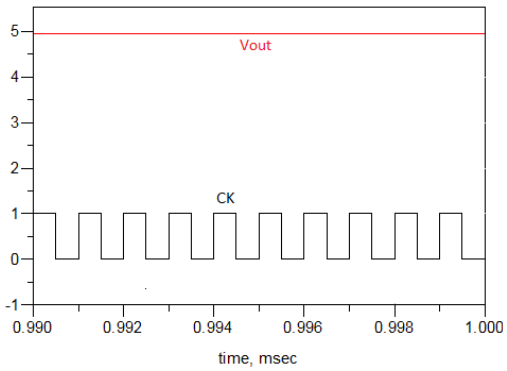


Fig.8: Clock signal and output voltage waveforms of the proposed charge pump

Figure 9 presents the output voltages of the simulated charge pump for various input voltages. The clock signal frequency is set to 1MHz. As it is clear from Figure 9, the increment of input voltage culminates in increasing output voltages of the charge pump, thus the relation of input and output voltages is approximately linear.

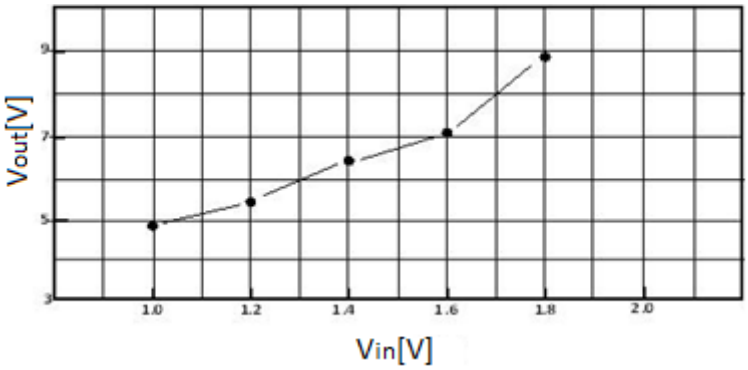


Fig.9: The output voltage versus different input voltages

The layout of the proposed charge pump is shown in Figure 10.

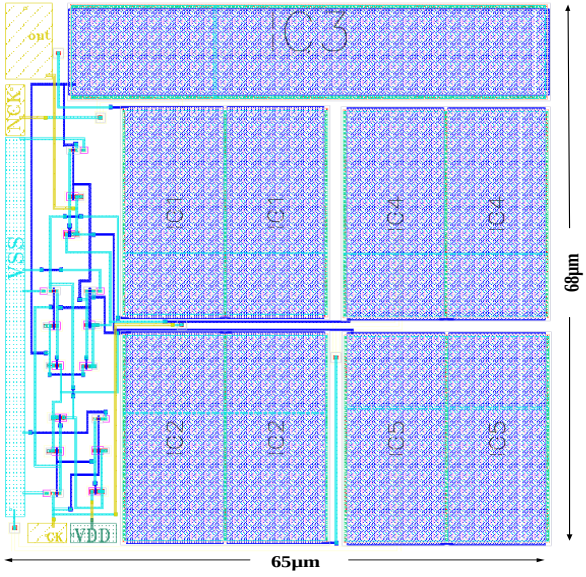


Fig.10: The layout of the proposed charge pump

Table 1 compares the characteristic of the proposed charge pump with the one other charge pump circuits. As it is clear from Table 1, the voltage conversion ratio of the proposed charge pump is significantly greater than the that of the other references. The proposed charge pump not only has better performance than the other circuits, but only has higher efficiency and lower chip area.

Table 1: The comparison of the proposed charge pump with the other charge pump circuits

| Ref | Process (nm) | Stage number | Input Voltage (V) | Output Voltage (V) | Conversion ratio(%) | Power efficiency(%) | Area ($mm^2$) |
|---|---|---|---|---|---|---|---|
| [1] | 180 | 4 | 1.8 | 5.95 | 66 | _ | 0.0024 |
| [9] | 350 | 4 | 1.8 | 8.2 | 91.1 | 62 | 0.56 |
| [10] | 180 | 8 | 1.2 | 76.09 | 78.2 | _ | _ |
| [11] | 180 | 4 | 1.8 | 10.1 | 93 | 50 | _ |
| This work | 180 | 4 | 1.8 | 8.9 | 98 | 85 | 0.00442 |

## 5. Conclusions

A novel charge pump circuit which includes one PMOS pass transistor, two MOSFET transistors as invertor and one capacitor, is presented. The comparison between Dickson charge pump and the proposed charge pump clarifies that the output voltage and the voltage conversion ratio of the designed circuit are significantly ameliorated. The proposed charge pump is simulated in 180nm CMOS technology, while its chip area is 68µm×65µm. The simulation results show that for 1.8 V input voltage, the output voltages of first to fourth stage are 3.6V, 5.4V, 7.1V and 8.9V, respectively.

## References

[1] KC Wei, MBI Reaz, MS Amin, J Jalil, LF Rahman. Design of a low voltage charge pump circuit for RFID tag. *IEEE International Conference on Semiconductor Electronics*, 2012; 203–206.

[2] MJ Uddin, MI Ibrahimy, MB Reza, AN Nodin. Design and application of radio frequency identification systems. *Journal of Scientific Research*, 2009; 33(3):438–453.

[3] A Ashry, K Sharaf and M Ibrahim. A Compact Low-Power UHF RFID Tag. *Microelectronics Journal*, 2009; 40(11): 1504-1513.

[4] D Maksimovic, S Dhar. Switched-capacitor DC-DC converters for low-power on-chip application. *IEEE Power Electronics Specialists Conference*, 1999; 45–59.

[5] JF Dickson. On-chip high-voltage generation in NMOS integrated circuits using an improved voltage multiplier technique. *IEEE Journal of Solid-State Circuits*, 1976; 11(3):374–378.

[6] LD sheng, ZX Cheng, D Kui, LS Zheng, HX Mei, L Yao, TQ Ling. New design of RF rectifier for passive UHF RFID. *Microelectronics Journal*, 2010; 41(1): 51-55.

[7] C Lauterbach, W Weber, D Romer. Charge sharing concept and new clocking scheme for power efficiency and electromagnetic emission improvement of boosted charge pumps. *IEEE Journal of Solid-State Circuits*, 2000; 35(5):719–723.

[8] WC Huang, J C cheng, and PC Liou. A charge pump circuit by using voltage-doubler as clock scheme. *IEEE Conference on Industrial Electronics and Applications*, 2009; 112–116.

[9] YS Hwang, DS Wu, HC Lin, J Chen, C Yu. A new inverter-based charge pump circuit with high conversion ratio and high power efficiency. *Microelectronics Journal*, 2011; 42(8): 982-987.

[10] R Roushan, D Modak, S Mondal, RP Paily. On chip high voltage single clock swing enhanced charge pump circuit in 0.18um technology. *IEEE International Conference on Power and Energy in NERIST*, 2012; 1–15.

[11] R Pelliconi, D Lezzi, A Baroni, M Pasotti, P L Rolandi. Power efficient charge pump in deep submicron standard CMOS technology. *IEEE Journal of Solid-State Circuits*, 2003; 38(6):1068–1071.